A high dynamic-range, low-noise focal plane readout for VLWIR applications implemented with current mode background subtraction

Guang Yang, Chao Sun, Timothy Shaw, Chris Wrigley, Pavani Peddada, Edward Blazejewski, and Bedabrata Pain

Advanced Imager and Focal Plane Technology Group
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109-8099
Tel: (818)-354-5462, Email: Guang.Yang@jpl.nasa.gov

ABSTRACT

Design and operation of an ultra-high dynamic-range, low noise CMOS focal plane readout circuit featuring in-pixel automatic background suppression is presented. high-background, VLWIR infrared readout applications. Designed for high-background, VLWIR detector readout, each readout unit cell uses an accurate dynamic current memory to subtract the dark pedestal in current domain to allow noise-limited measurement of signals 85 dB below the dark level. The readout circuit is designed to operate at low-power dissipation, with high linearity, and is capable of handling pedestal currents upto 300 nA. The accurate background subtraction enables a very high effective charge handling capacity of over $5x10^9$ charges/pixel.

Keywords: large dynamic range, high background, QWIP, focal plane arrays, readout electronics, background suppression, signal handling capacity, current memory, buffered direct injection

1. INTRODUCTION

IR imaging systems that operate in the very long wavelength (VLWIR) region (12-18 μm) are required for a number of space-based applications such as monitoring the global atmospheric temperature profiles, relative humidity profiles, cloud characteristics, and the distribution of minor constituents in the atmosphere which are being planned for NASA's Earth Observing Systems. Imaging in VLWIR region presents several design problems, primarily to the presence of large background and detector dark levels. Enormous signal handling capacity and extremely small signal to background contrast imposes stringent challenges to focal plane readout design. In this paper, design and operation of a readout circuit for a atmospheric sounder instrument operating in VLWIR region is presented. The paper is organized as follows. In section 2, the instrument focal plane specifications and associated design challenges are described. In section 3, the readout circuit implementation and design considerations are presented. In section 4, test results from the prototype readout circuit is presented, followed by conclusion in section 5.

2. INSTRUMENT FOCAL PALNE SPECIFICATIONS

The focal plane readout circuit is designed for operation in an atmospheric sounding instrument called Integrated Multispectral Atmospheric Sounder (IMAS) that is expected to fly on the NASA EOS-PM1 mission. IMAS is an integrated, low-power, low-mass instrument approach capable of measurements in visible, infrared, microwave wavebands. The infrared spectrometer subsystem collects data in the range from 3.74 μm to 15.4 μm and provides the primary sounding information. IMAS will enhance global weather forecasting by NOAA and the Global Research Program of NASA's Mission to Planet Earth by improving numerical weather prediction, predicting seasonal-to-interannual effects of El Nino and other transient climate anomalies, characterizing the optical

properties of the atmospheric constituents, and monitoring variations and trends in global energy and water cycles.

The IMAS infrared sounder will cover a wide spectral region from MWIR (3.7 μm) to VLWIR (15.4 μm) with a spectral resolving power of about 1200. Spectral data is acquired by means of a grating spectrometer and cooled (55K to 65K) Quantum Well Infrared Photodetector (QWIP) arrays. These devices demonstrate extremely uniform response, exhibit low 1/f noise, are defect free, reproducible, and low cost, and readily lend themselves to two-dimensional arrays. The specification of the IMAS system is listed in Table 1.

Very Long Wavelength IR Detector	Quantum Well Infrared Photodetector (QWIP)
Detector Material	GaAs/AlGaAs Superlattice
Optical Coupling	Slotted Grating
Array Configuration	2 x 130
Unit Cell Size	50 μm x 400 μm
Focal Plane Type	Direct Hybrid
Temperature of Operation	55 ^{o}K
Wavelength Band	14.67 to 15.4 μm (M12)
Detectivity (D*) (Required)	1.1×10^{11} $cm\sqrt{Hz}/W$ ($NE\Delta T$ = 0.35 ^{o}K)
Exposure Time	1.4 $msec$

Table 1. *Specifications of IMAS focal plane*

There are several challenges in the design of readout circuit to meet the requirements of the IMAS system.

1. The QWIP used by the IMAS system has low output impedance. The measured impedance of QWIP detector is a 10 MΩ resistance in parallel with a 0.5 pF capacitance. In order to achieve high injection efficiency, the readout circuit must have low input impedance compared to the detector.
2. The IMAS system has a very large background level. At the operation temperature of 55 °K, the detector leakage current of QWIP is about 100 to 300 nA, and the scene background photon induced dark current is about 3.5 nA. For the integration time of 1.4 msec, the total dark level is 10^9 to 3×10^9 e^-/pixel. Thus, the readout circuit is required to have a large signal handling capacity.
3. Because of the high detector leakage, the noise limit is governed by the shot noise in the detector dark current. For a QWIP with a photoconductive gain of around 0.1, the typical QWIP noise limit is around 10 pA (correspondingly 6×10^4 e^-/pixel) for the same exposure time. In other words, the focal plane contrast (defined as the ratio of the minimum detectable signal to the background level) is extremely small. The readout circuit needs to be both accurate and quiet (low-noise) enough to accurately measure a differential signal that could be as high as 85 dB below the dark level.

The high background level imposes a conflicting design requirement on the readout circuit. In order to directly handle a large background a large capacitor is needed on the focal plane. This capacitance is estimated to be around 150 pF, which is practical from a CMOS focal plane readout circuit design standpoint. However, even if such a capacitor could be incorporated on the focal plane, circuit noise will be too high to meet the noise requirement. In this paper, a novel readout circuit that simultaneously handles large background pedestal and is capable of measuring a small differential signal riding on top of the pedestal is reported. The circuit uses in-pixel current mode background subtraction to extend the dynamic range while providing low read noise.

3. READOUT CIRCUIT IMPLEMENTATION

The readout focal plane consists of a bilinear array of 2x132 multiplexers, with the unit cell consisting of a

buffered direct injection (BDI) input, a current-mode pedestal subtracting circuit, and a double-sampled differential readout (DSDR) – shown schematically in Figure 1. Schematically, the QWIP detector is represented by a current source parallel with a variable resistor and a capacitor. The BDI input circuit provides both the required bias stability for the QWIP and a high input impedance that enables high quantum efficiency. The current mode pedestal subtracting circuit is comprised of a cascode current memory with switch-feedthrough reduction as shown in Figure 2, and an isolation FET (M_{read}). The current memory operates as follows. When clock ϕ_1 goes high, the gate voltage of the memory transistor (M_{mem}) charges up to a value such that the current flowing through M_{mem} is equal to the current flowing into its drain. When ϕ_1 goes low, the gate voltage is sampled and held, so that the dynamic current memory provides a current equal to the current memorized. In this design, two techniques are used to reduce the effects of switch feedthrough. First, a dummy switching transistor is used to compensate for the channel charge under the FET being shut-off. Secondly, a capacitively-coupled second memorization loop is added that suppresses the switch-feedthrough voltage by the ratio of C_1 to C_2. The ratio is designed to be around 100, which makes the error due to switch-feedthrough insignificant.

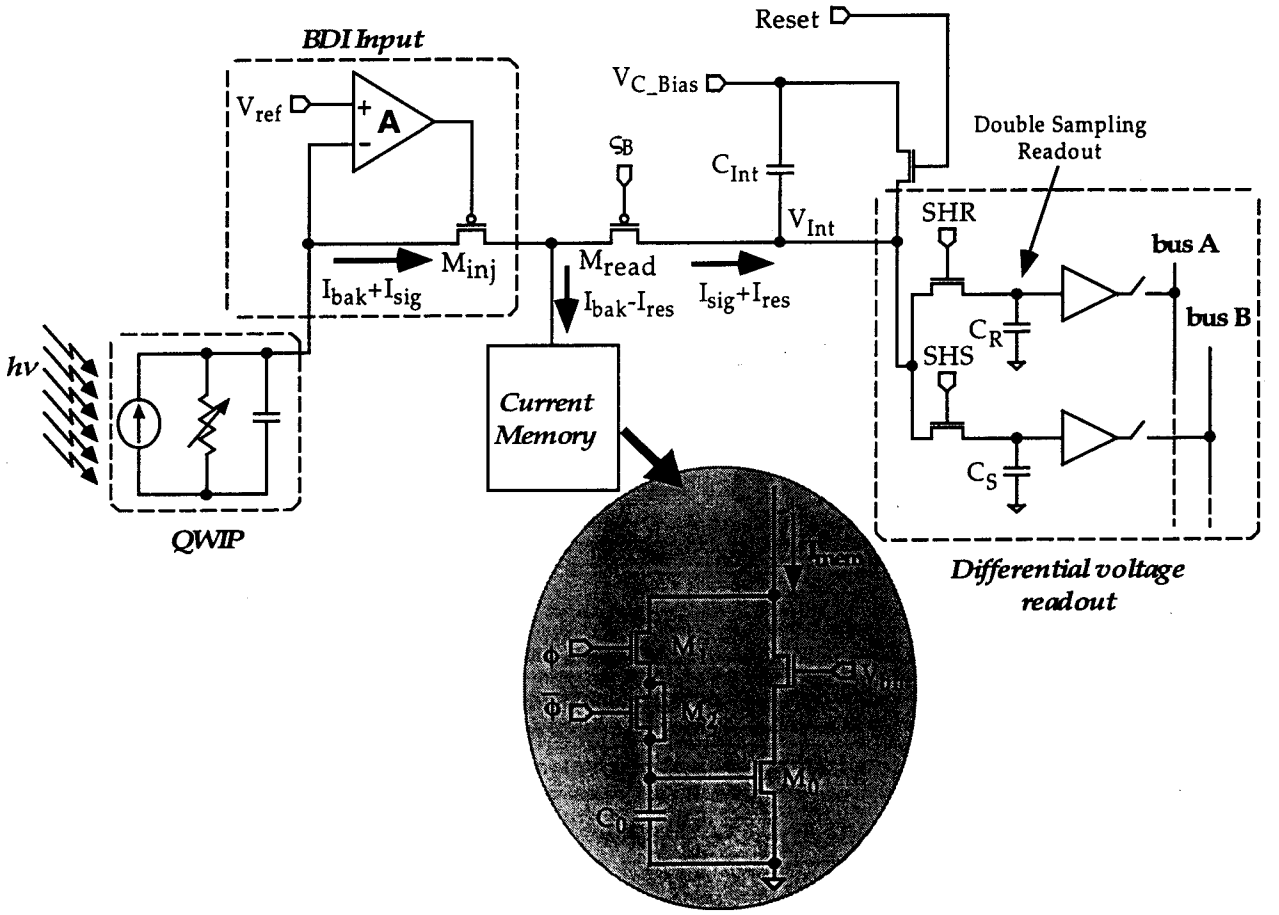


Figure 1. *Circuit implementation of IR readout with current mode background subtraction.*

The circuit performs automatic dark level suppression by first sampling and holding the dark level during the calibration cycle, and then subtracting the same during the imaging phase. Unlike other background suppression techniques, most of the background estimation and subtraction is carried out in the current mode. This allows the circuit to effectively operate with variable gains: low gain for the background, and a high gain for the differential signal enabling low noise performance. The readout circuit operates as follows.

During the calibration cycle, the current I_{bak} flowing through each QWIP consists of the detector dark current as well as the current due to scene and instrument background ($I_{bak} = I_{dark\text{-}QWIP} + I_{scene\text{-}back}$). The pedestal due to this current I_{bak} is measured and sampled in two steps. First, the current memory is enabled to memorize both the scene and instrument background, as well as the detector dark current. In the present application, the detector dark current is the dominant component, being around 100-300 nA, and the scene background is an order of magnitude lower. After the memorization phase is over, ideally the total dark current (I_{bak}) is equal to the current (I_{mem}) flowing through M_{mem} during the memory read phase. However, due to circuit imperfections, these two currents are not equal, causing an error current $I_{res} = I_{bak} - I_{mem}$ to flow. The pedestal due to the error current is then estimated in the voltage mode by integrating the error current on the integration capacitor (C_{Int}), and sampling the resultant voltage onto one of the capacitors (C_R) of the DSDR as shown in Figure 1. This completes the dark level memorization phase.

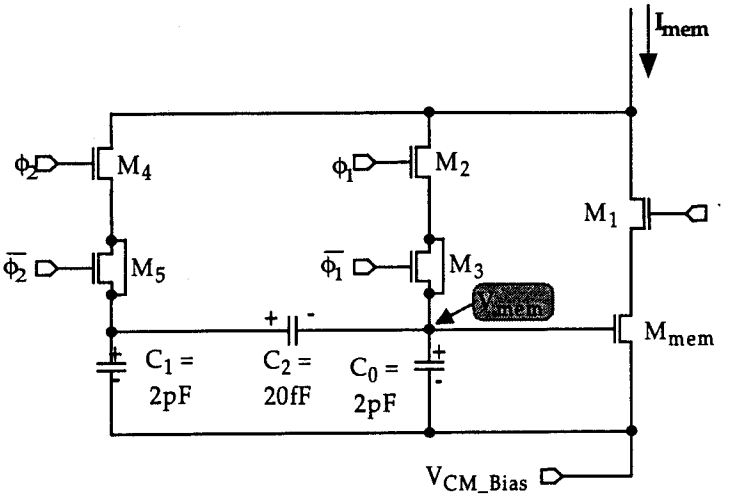


Figure 2. *Current memory with feed back suppression.*

The calibration cycle is followed by imaging phase during which the QWIP current is increased by I_{sig} - the infrared signal to be measured. The current memory subtracts most of the background, and sends the signal (I_{sig}) plus an offset current (I_{res}) to the integration node. After the exposure is over, the resultant voltage is sampled on the other capacitor (C_S) in the DSDR. The difference between the potential of the two capacitors is then proportional to the infrared signal (I_{sig}), while the background is suppressed by over 4 orders of magnitude. The gate voltage of isolation FET M_{read} (ϕ_{read} in Figure 1) is DC biased such that during calibration cycle, the current memory potential shuts M_{read} off, while during the imaging phase, the source of M_{read} charges up to a potential that allows the current to be injected into the integration capacitance. Operation of the circuit without pulsing ϕ_{read} is important since it prevents injection of switching noise into a sensitive node.

It is important to maintain high injection efficiency at the current memory interface node (V_{read}) in order to achieve high conversion gain and low noise. The current flowing from the left of the node V_{read} ($I_{bak}+I_{sig}$) to its right ($I_{sig}+I_{res}$) may vary by over three orders of magnitude (see figure 1), causing an decrease in the conductance at the source of M_{read}, and leading to a reduction in the injection efficiency. To maintain high injection efficiency, two conditions need to be satisfied. The effective conductance (g_{inj}) looking into the left of the node must be much smaller than the combined conductance of the current memory output conductance (g_{CM}) and conductance at the source of M_{read} (g_{mread}). Secondly, g_{CM} must be much smaller than g_{mread}, in order to ensure that the differential current is injected into the source of M_{read}, and not into the current memory. The total injection efficiency at the current memory interface node may be expressed as:

$$\eta_{inj} = \frac{g_{mread}(1+A)A_1R_{det}}{1+(g_{CM}+g_{mread})(1+A)A_1R_{det}} \quad (1)$$

where, A_1 is the gain of BDI op-amp, A is the intrinsic gain of injection FET M_{inj}. The readout circuit is designed with a cascode current memory to restrict g_{CM} to a small value, while the open loop gain of the BDI op-amp can

be chosen to be sufficiently high to reduce the value of g_{inj}, so that the total injection efficiency is high. For I_{sig} three orders of magnitude below I_{bak}, an op-amp gain of 300 is sufficient to achieve an injection efficiency greater than 0.99. A op-amp with gain of 300 can be readily designed in available CMOS technology, enabling the readout circuit implementation with high linearity and gain differential gain.

3. EXPERIMENT SETUP AND TEST RESULTS

The test chips were fabricated using Hewlett Packard (HP) 1.2 μm single poly-silicon, double metal process. The photographs of readout circuit testing chips are shown in Figure 3.

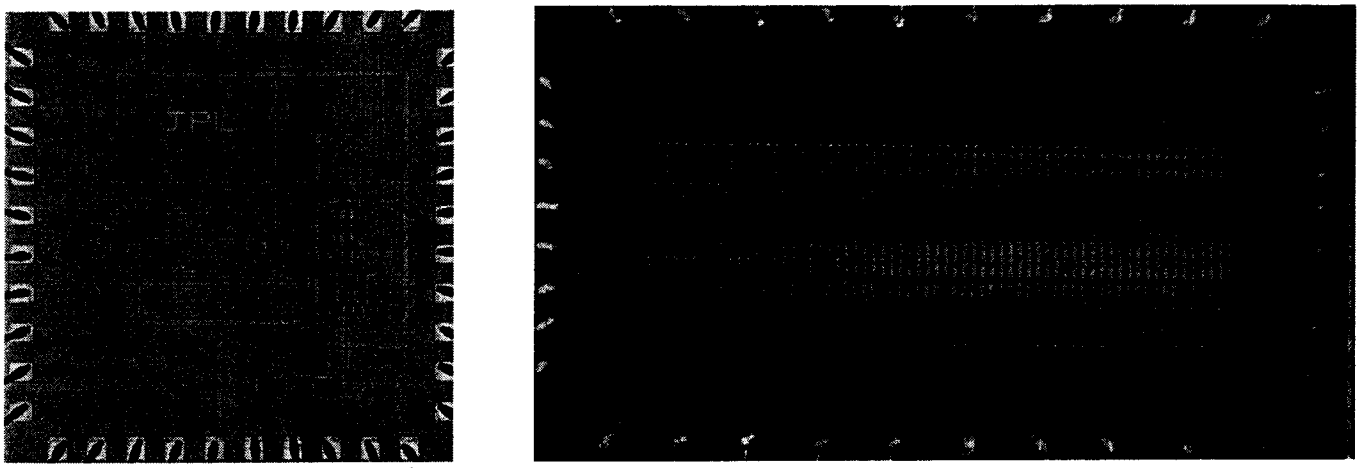


Fig 3a *Fig 3b*

Figure 3. *Photographs of readout circuit testing chips: 3a Pixel test chip; 3b 1x65 array chip*

The experimental set-up that allows independent evaluation of the performance of readout circuit is shown in figure 4. In order to mimic the QWIP detector as closely as possible, and in order to inject a low noise current, a resistive network is used. The network consists of a resisitve divider that allows injection of a d.c. bias current, and small modulation current (generated by a pulsed voltage source) whose value depends on the resistive division and the amplitude of the pulsed source, as shown in figure 4. While the array chip shown in figure 3b is functional, most of the data reported is taken from the pixel test chip for ease of operation. Most of the data is taken at near room temperature, due to a problem with the cryogenic dewar. This is not a problem, since functionally, it is more difficult to operate the circuit at room temperature.

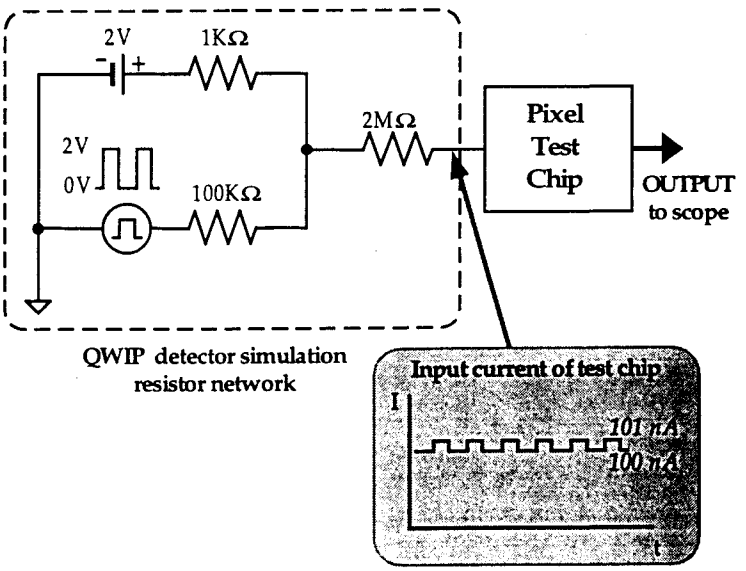
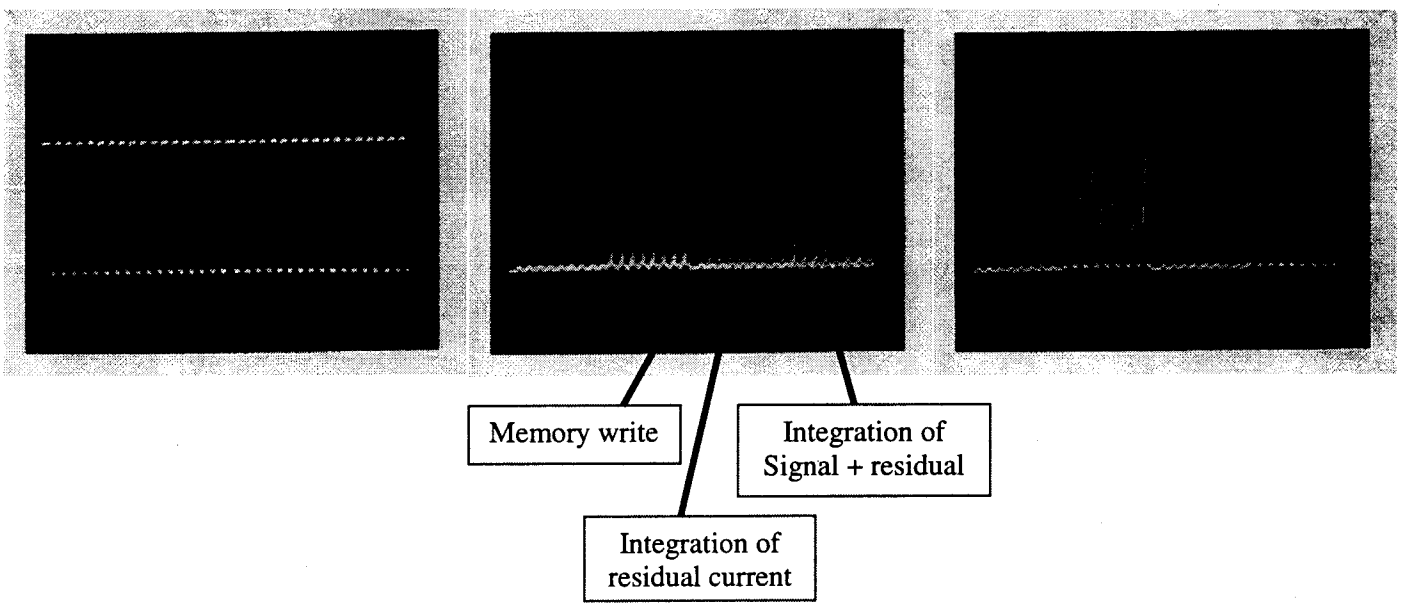


Figure 4. *Experimental setup of test chip.*

3A. Demonstration of background suppression

Figure 5 shows the pictures of scope screen when the scope was measuring the voltage output of pixel test chip output at the integration node (V_{Int} in Figure 1). The scale of the scope was set to 1 V per division in y-direction and 5

msec per division in x-direction. Integration time on node V_{Int} was set to about 1 msec. Figure 5(a) shows the signal without current subtraction (with current memory turned off by setting V_{bn} in Figure 2 to ground). We can see the output voltage raising rapidly after the reset pulse turn off. It indicated that 100 nA of pedestal current will charge up the integration capacitor (V_{Int} in Figure 1) very fast. Figure 5(b) shows the image of 100 pA signal on 100 nA pedestal current with current subtraction operation. It demonstrated that with the current subtraction operation, the residual current, which is caused by the error of current memory, is in the same order of a 100 pA signal. That indicated that the residual error is about 0.1% of pedestal current. As a comparison, Figure 5(c) shows the image of 1 nA signal on 100 nA pedestal current with current subtraction operation.



(a) Image of signal without current subtraction;

(b) Image of 100 pA signal on 100 nA pedestal;

(c) Image of 1 nA signal on 100 nA pedestal;

Figure 5. *Demonstration of background current subtraction.*

B. Current memory leakage

By using standard CMOS process with linear capacitor option, the leakage of capacitor will cause the error in current memory. As shown in Figure 2, the leakage of capacitors C_1, C_2, and C_3 will reduce the memorized voltage V_{mem}. As a result, the memorized current I_{mem} will decrease which will cause the increase of signal current and the output voltage V_{Int} in Figure 1. However, the leakage of capacitor will reduce rapidly as the operation temperature decrease. The comparison of current memory leakage at room and low temperature is shown in Figure 6. This experiment was done by sending a constant current of 100 nA to the test chip with background current subtraction operation. Inspection of this figure shows that the output voltage increases to its saturation level in about 1200 msec with a slope of 0.2 mV/msec. However, at low temperature of about –20 °C, the output voltage increases slightly with a slope of 0.08 mV/msec. For the operation of about 55 °K, current memory leakage will be very small and the variation of I_{mem} will be insignificant.

C. Readout Linearity

The linearity of the readout voltage vs. input signal current was measured under room temperature. This measurement carried out by memorizing pedestal current I_{mem} during calibration period and providing an additional signal current I_{sig} during the readout period. Measurement carried out for different I_{mem} from 10 nA to 200 nA. And the input signal changed from 10 pA to 100 pA. Figure 7 gives the output voltage V_{out} as a function of input signal I_{sig} with 100 nA background subtraction. The measured number of integration capacitor C_{Int} was 2.8 pF, and the conversion gain equals to 0.05 $\mu V/e^-$. The tested data also gave the linearity was greater than 99%.

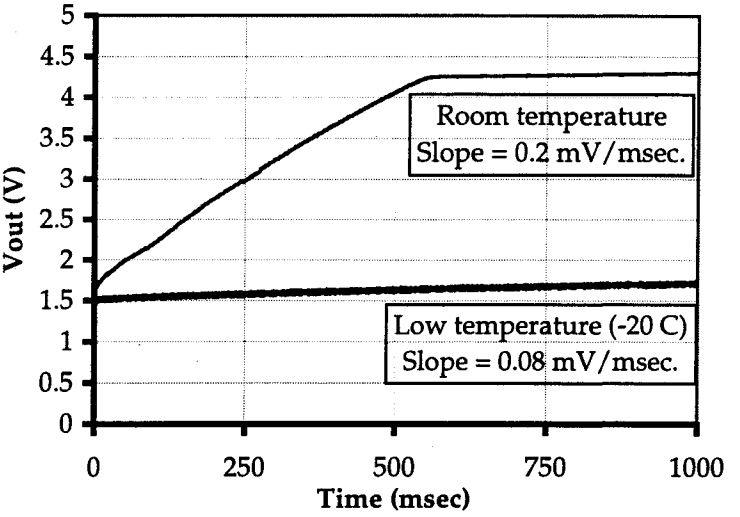


Figure 6. *Comparison of current memory leakage at room and low temperature.*

D. Read noise

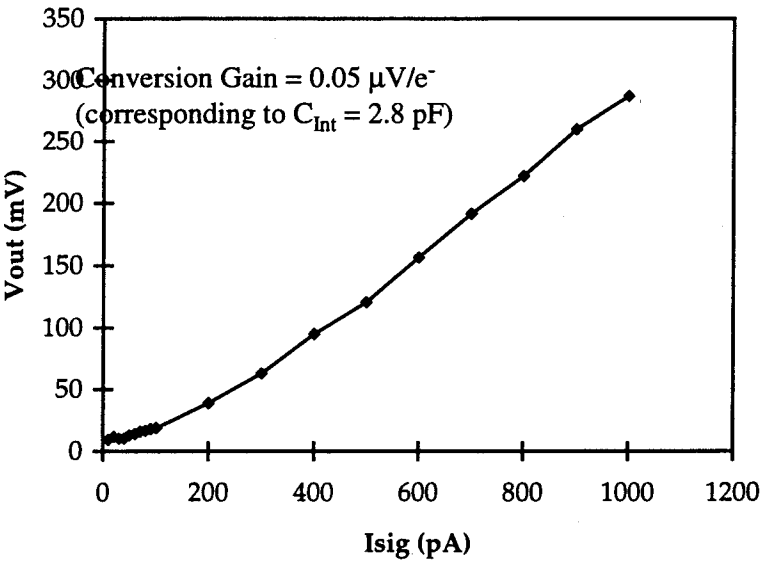


Figure 7. *Output voltage vs. input signal with 100 nA background current subtraction.*

A detail noise analysis on the readout circuit conducted by B. Pain (see paper 3360-06 in this preceding) shows that, the noise power at the integration node (V_{Int} in Figure 1) is given by:

$$\langle V_0^2 \rangle = \left[2qqI + \frac{KT}{R_{det}} (1 + g_{mm} R_{det}) \right] \frac{t_{int}}{C_{int}^2}. \qquad (2)$$

Where, g is the gain of photoconductor, R_{det} is the detector resistance, and g_{mm} is the transconductance of current memory transistor. The plot of readout noise as a function of memorized current is shown in Figure 8. Inspection of this figure shows that the measured noise is good agree with the above model. In additional, the measured noise shows expected square root dependence on memorized current. It implies that in real device operation, detector dark current shot noise limits the system readout noise.

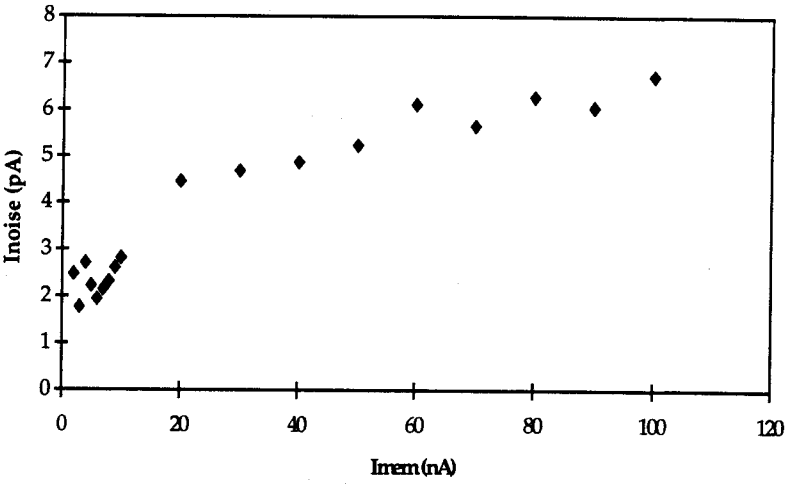
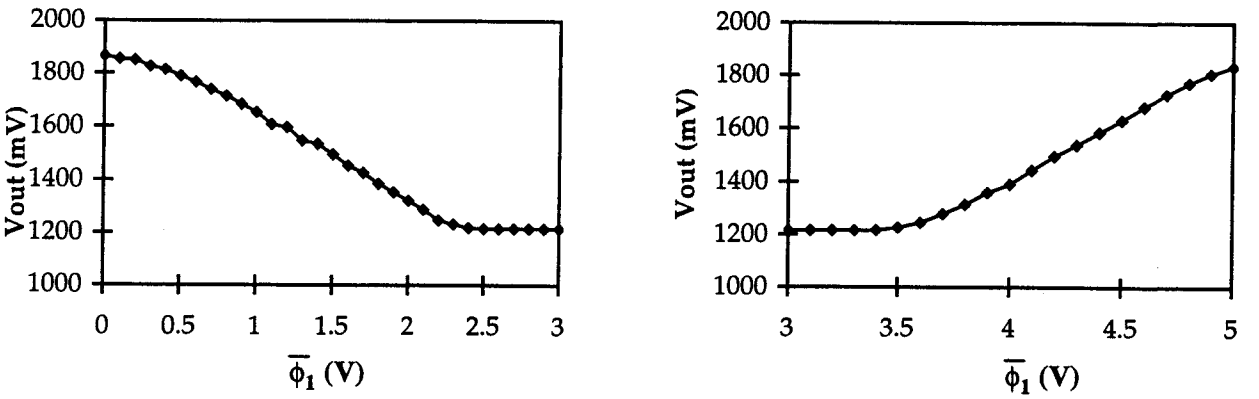


Figure 8. *Readout noise as a function of memorized current.*

E. Current memorization accuracy

The accuracy of current memory is determined by the switch feedthroughs of two switch pairs in current memory —ϕ_1 and $\bar{\phi}_1$, ϕ_2 and $\bar{\phi}_2$. According to the experiments, the accuracy of current memory as well as the output voltage depends more on ϕ_1 and $\bar{\phi}_1$. However, as the voltage swing of $\bar{\phi}_1$ in the certain region, the output voltage has its minimal dependence of memorization error. Figure 9 shows the



(a) $\bar{\phi}_1$ swing from 0 V to $\bar{\phi}_1$-Hi. (b) *$\bar{\phi}_1$ swing from $\bar{\phi}_1$-Lo to 5 V.*

Figure 9. *Output voltage as function of $\bar{\phi}_1$ voltage swing when ϕ_1 swing from 0 to 5 volts.*

output voltage as a function of voltage swing on $\bar{\phi}_1$ when ϕ_1 was swinging from 0 to 5 volts. Where, Figure 9(a) shows $\bar{\phi}_1$ swings from 0 V to $\bar{\phi}_1$-Hi, and $\bar{\phi}_1$-Hi was various from 0 to 3 V; Figure 9(b) shows $\bar{\phi}_1$ swings from $\bar{\phi}_1$-Lo to 5 V, and $\bar{\phi}_1$-Li was various from 3 to 5 V. Inspection of this figure shows that when the voltage swing of ϕ_1 was from 0 to 5 V, a minimal dependence of memorization error can be achieved for $\bar{\phi}_1$ has a voltage swing from 0 V to $\bar{\phi}_1$-Hi between 2.25 and 3 V, and for $\bar{\phi}_1$ has a voltage swing from $\bar{\phi}_1$-Li between 3 and 3.5 V to 5 V. This experimental result indicates the array operation feasibility of the readout circuit.

The summary of the design aspects and experimental results of the VLWIR readout circuit is given in Table 2.

Table 2. *Summary of VLWIR readout circuit.*

Circuit implemtation	Buffered direct injection input; Current mode pedestal subtraction by using current memory with switch-feedthrough reduction; Double sampling differential readout.
Array configuration	2 x 130
Pixel size	50 μm x 400 μm
Injection capacitor	2.8 pF
Linearity	> 99% (as measured after in-pixel dark level suppression
Current memory error	0.1%
Read noise	5.6 pA @ 100 nA back ground and 1 msec exposure $\rightarrow 3.4 \times 10^4$ e^-/exposure (2×10^4 smaller than background)
Minimum signal measured	10 pA
Background handing capacity	10^7 to 1.25×10^9 e^-
Contrast handling capacity	100 dB below background

5. CONCLUSIONS

A high dynamic-range, low noise CMOS focal plane readout array has been designed and fabricated. The readout circuit has been designed for the application of very long wavelength (12-18 μm) IR signal. The readout unit cell consisting of a buffered direct injection input, a current-mode pedestal subtracting circuit, and a double-sampled differential readout. The characteristics of a single readout cell have been tested. This work first demonstrated low noise, accurate current subtraction readout for high leakage (or high background) infrared detection. Preliminary experimental results indicate the capability of background suppression four orders of magnitude. Continuous work is on the cyro-temperature operation of the designed circuit.

6. AKNOWLEDEGEMTS

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, and was jointly sponsored Goddard Space Flight Center, and the National Aeronautics and Space Administration, Office of Space Science. The authors would like to give the special thanks to Dr. Eric Fossum at Photobit LLC for his valuable discussions, and special thanks to Dr. Tom Cunningham, Mr. Mike Fitzsimmons, Mr. John Koehler, and Mr. Monico Ortiz for their help.